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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,560	10/01/2003	Michael Lee Workman	Pillar 716	3994

7590 03/31/2005

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EXAMINER	
PARK, ILWOO	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,560	WORKMAN ET AL.	
	Examiner	Art Unit	
	Ilwoo Park	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *8-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 22 and 23 are amended. El-Batal et al., Okada, Cargemel et al., Walker, and Pinson were cited in the last office action. The following rejections now apply. Group I (claims 1-7, 22 and 23) is elected without traverse. Claims 1-7, 22 and 23 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over El-Batal et al., US patent application publication No. US 2003/0221061 A1, and Bicknell et al., US patent application publication No. US 2003/0193776 A1.

As to claims 1 and 23, As to claim 1, El-Batal et al teach each of a plurality of coupling circuits for an ATA storage device, comprising:

a first Serial ATA controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 760 of fig. 7A] receiving a first Serial ATA communication path;

a second Serial ATA controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 761 of fig. 7A] receiving a second Serial ATA communication path;

a Serial ATA device-side transceiver [e.g., analog front end 601 of fig. 6 at the storage device 742 in order to transmit and receive serialized datastream to and from the physical layer interfaces at the controllers side; disks are Serial ATA disks which are inputting and outputting serialized datastream in accordance with a Serial ATA Specification in paragraph 0051]; and

coupling circuit switches [e.g., multiplexer 741] which selectively coupling either the first Serial ATA controller-side transceiver or the second Serial ATA controller-side transceiver to the Serial ATA device-side transceiver based on the logic state of a path control line.

However, El-Batal et al do not expressly disclose a microcontroller in the coupling circuit adapted to control the coupling circuit switches for the selective path connection. Bicknell et al teach a coupling circuit [mux 208 in figs 6-8] each associated with each of Serial ATA disks for selectively coupling a Serial ATA communication path of each Serial ATA disk with a Serial ATA path of one of multiple controllers [controllers 1, 2] by a microcontroller [micro-computer 222 in fig. 8; paragraph 0028] in the coupling circuit adapted to control the coupling circuit switches for the Serial ATA connection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of El-Batal et al and Bicknell et al because they both teach coupling circuit switches in a coupling circuit for selectively coupling a Serial ATA communication path of each Serial ATA disk with a Serial ATA path of one of multiple controllers and the Bicknell et al's teaching of a microcontroller in the coupling circuit adapted to control the coupling circuit switches for the Serial ATA

connection would increase feasibility of Serial ATA communication path control between the two controllers and a Serial ATA disk of El-Batal et al.

4. Claims 1, 3, 4, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over El-Batal et al., US patent application publication No. US 2003/0221061 A1, and Steinmetz et al., US patent application publication No. US 2004/0139260 A1.

As to claims 1 and 23, As to claim 1, El-Batal et al teach each of a plurality of coupling circuits for an ATA storage device, comprising:

a first Serial ATA controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 760 of fig. 7A] receiving a first Serial ATA communication path;

a second Serial ATA controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 761 of fig. 7A] receiving a second Serial ATA communication path;

a Serial ATA device-side transceiver [e.g., analog front end 601 of fig. 6 at the storage device 742 in order to transmit and receive serialized datastream to and from the physical layer interfaces at the controllers side; disks are Serial ATA disks which are inputting and outputting serialized datastream in accordance with a Serial ATA Specification in paragraph 0051]; and

coupling circuit switches [e.g., multiplexer 741] which selectively coupling either the first Serial ATA controller-side transceiver or the second Serial ATA controller-side

transceiver to the Serial ATA device-side transceiver based on the logic state of a path control line.

However, El-Batal et al do not expressly disclose a microcontroller in the coupling circuit adapted to control the coupling circuit switches for the selective path connection. Steinmetz et al teach a coupling circuit [path controller card] associated with a Serial ATA disk for selectively coupling a Serial ATA communication path of each Serial ATA disk with a Serial ATA path of one of multiple controllers [storage-shelf routers] by a microcontroller [micro-controller 1418 in fig. 14B; paragraph 0099] in the coupling circuit adapted to control the coupling circuit switches [2:1 MUX 1412] for the Serial ATA connection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of El-Batal et al and Steinmetz et al because they both teach coupling circuit switches in a coupling circuit for selectively coupling a Serial ATA communication path of each Serial ATA disk with a Serial ATA path of one of multiple controllers and the Bicknell et al's teaching of a microcontroller in the coupling circuit adapted to control the coupling circuit switches for the Serial ATA connection would increase feasibility of Serial ATA communication path control between the two controllers and a Serial ATA disk of El-Batal et al.

As to claim 3, Steinmetz et al teach the microcontroller includes a processor coupled to a power switch and coupled to the coupling circuit switches [fig. 14B].

As to claim 4, Steinmetz et al teach the microcontroller includes a processor coupled to a power switch and coupled to the coupling circuit switches; however, El-Batal et al and Steinmetz et al do not disclose a set of logics including a set of D flip-

flops. It is well known in the art that a set of logics including a set of D flip-flops for simplicity in order to latch a control signal from the microcontroller to simply eliminate burden of the microcontroller maintaining the control signal at the same level until next path change.

As to claim 22, El-Batal et al teach each of a plurality of coupling circuits for an ATA storage device, comprising:

a first controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 760 of fig. 7A] receiving a first communication path;

a second controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 761 of fig. 7A] receiving a second communication path;

a storage device-side transceiver [e.g., analog front end 601 of fig. 6 at the storage device 742 in order to transmit and receive serialized datastream to and from the physical layer interfaces at the controllers side; disks are Serial ATA disks which are inputting and outputting serialized datastream in accordance with a Serial ATA Specification in paragraph 0051]; and

coupling circuit switches [e.g., multiplexer 741] which selectively coupling either the first controller-side transceiver or the second controller-side transceiver to the Serial ATA device-side transceiver based on the logic state of a path control line.

However, El-Batal et al do not expressly disclose a microcontroller in the coupling circuit adapted to control the coupling circuit switches for the selective path connection and control the power to the storage. Steinmetz et al teach a microcontroller [micro-controller 1418 in fig. 14B; paragraph 0099] in a coupling circuit [path controller

card] adapted to control the coupling circuit switches [2:1 MUX 1412] for the selective path connection between one of multiple controllers [storage-shelf routers] and a storage device and control the power to the storage. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of El-Batal et al and Steinmetz et al because they both teach coupling circuit switches in a coupling circuit for selectively coupling a communication path between one of multiple controllers and a storage and the Steinmetz et al's teaching of a microcontroller in the coupling circuit adapted to control the coupling circuit switches for the communication path connection would increase feasibility of communication path control between the two controllers and a storage device of El-Batal et al and Steinmetz et al's teaching of the microcontroller in the coupling circuit further adapted to control the power to the storage device would further increase user friendliness of repairing the failed storage device.

5. Claims 3-7 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over El-Batal et al and Bicknell et al as applied to claim 1 above, and further in view of Cargemel et al., US patent No. 6,295,609.

As to claim 3, El-Batal et al and Bicknell et al teach do not disclose the microcontroller includes a processor coupled to the coupling circuit switches. However, El-Batal et al and Bicknell et al do not disclose the microcontroller includes a processor coupled to a power switch. Cargemel et al teach a microcontroller includes a processor controlling the power to the storage device [fig. 2; col. 6, line 55-col. 7, line 10]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to implement the Cargemel et al's teaching of a microcontroller includes a processor controlling the power to the storage device into the microcontroller of El-Batal et al and Bicknell et al in order to increase user friendliness of repairing the failed storage device.

As to claim 4, El-Batal et al and Bicknell et al teach the microcontroller includes a processor coupled to a power switch and coupled to the coupling circuit switches; however, El-Batal et al and Bicknell et al do not disclose a set of logics including a set of D flip-flops. It is well known in the art that a set of logics including a set of D flip-flops for simplicity in order to latch a control signal from the microcontroller to simply eliminate burden of the microcontroller maintaining the control signal at the same level until next path change.

As to claims 5 and 22, El-Batal et al and Bicknell et al teach the microcontroller is programmed to as follows switch the coupling circuit to a first storage controller; and switch the coupling circuit to a second storage controller. However, El-Batal et al and Bicknell et al do not disclose power up the storage device; and power down the storage device. Cargemel et al teach [col. 5, lines 3-19; col. 6, line 55-col. 7, line 11] the microcontroller is programmed to as follows: switch the coupling circuit to a first storage controller; switch the coupling circuit to a second storage controller; power up the storage device; and power down the storage device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the Cargemel et al's teaching of a microcontroller controlling power up/down

the storage device into the microcontroller of El-Batal et al and Bicknell et al in order to increase user friendliness of repairing the failed storage device.

As to claim 6, Cargemel et al teach [col. 6, line 55-col. 7, line 11] the microcontroller further programmed to as follows: write data to a memory; read data from the memory; and read the status of the coupling circuit.

As to claim 7, Cargemel et al teach [col. 4, lines 7-13; col. 5, lines 3-19; col. 6, line 55-col. 7, line 11] the status includes information on whether the storage is coupled to the first controller-side or the second controller-side, the storage is powered up or down, the communication status, and/or the board revision and code revision levels of the coupling circuit.

6. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over El-Batal et al and Steinmetz et al as applied to claim 1 above, and further in view of Cargemel et al., US patent No. 6,295,609

As to claim 5, El-Batal et al and Steinmetz et al teach the microcontroller is programmed to as follows switch the coupling circuit to a first storage controller; and switch the coupling circuit to a second storage controller. However, El-Batal et al and Steinmetz et al do not disclose power up the storage device; and power down the storage device. Cargemel et al teach [col. 5, lines 3-19; col. 6, line 55-col. 7, line 11] the microcontroller is programmed to as follows: switch the coupling circuit to a first storage controller; switch the coupling circuit to a second storage controller; power up the storage device; and power down the storage device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

implement the Cargemel et al's teaching of a microcontroller controlling power up/down the storage device into the microcontroller of El-Batal et al and Steinmetz et al in order to increase user friendliness of repairing the failed storage device.

7. As to claim 6, Cargemel et al teach [col. 6, line 55-col. 7, line 11] the microcontroller further programmed to as follows: write data to a memory; read data from the memory; and read the status of the coupling circuit.

8. As to claim 7, Cargemel et al teach [col. 4, lines 7-13; col. 5, lines 3-19; col. 6, line 55-col. 7, line 11] the status includes information on whether the storage is coupled to the first controller-side or the second controller-side, the storage is powered up or down, the communication status, and/or the board revision and code revision levels of the coupling circuit.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over El-Batal et al. and Bicknell et al. as applied to claim 1 above, and further in view of Deyring et al., US patent application publication No. US 2003/0158991 A1.

As to claim 2, El-Batal et al and Bicknell et al teach a Serial ATA Specification [in Physical Layer Section; paragraph 0005 of El-Batal et al] requires Out Of Band (OOB) signals need to be sent and received at each transceivers in order to detect COMRESET, COMINIT, and COMWAKE during a Serial ATA bus operation. However, El-Batal et al and Bicknell et al do not expressly disclose activating the first Serial ATA controller-side transceiver, the second Serial ATA controller-side transceiver, and the Serial ATA storage device-side transceiver. Deyring et al teach an out of band squelch control component sending and receiving Out Of Band (OOB) signals sent and received

at a transceiver by activating [figs. 1 and 5] the transceiver for a Serial ATA bus operation; and Deyring et al further teach [paragraph 0004] each transceiver is required at each end of the Serial ATA bus. Therefore, it would have been obvious to one of ordinary skill in the art of a Serial ATA bus operation at the time the invention was made to combine the teachings of El-Batal et al, Bicknell et al, and Deyring et al because they both teach a Serial ATA bus operation according to Serial ATA Specification and the Deyring et al's teaching of an out of band squelch control component activating each transceiver in order to send and receive OOB signals for a bus synchronization would increase reliability of El-Batal et al and Bicknell et al's Serial ATA bus operation.

Conclusion

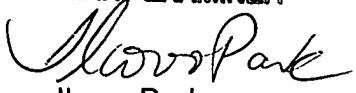
10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (571) 272-4155. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (571) 272-4146. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER



Ilwoo Park

March 28, 2005